

FIG. 1
 (PRIOR ART)

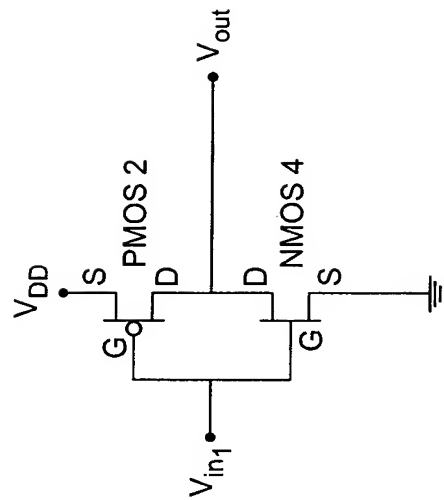


FIG. 2
 (PRIOR ART)

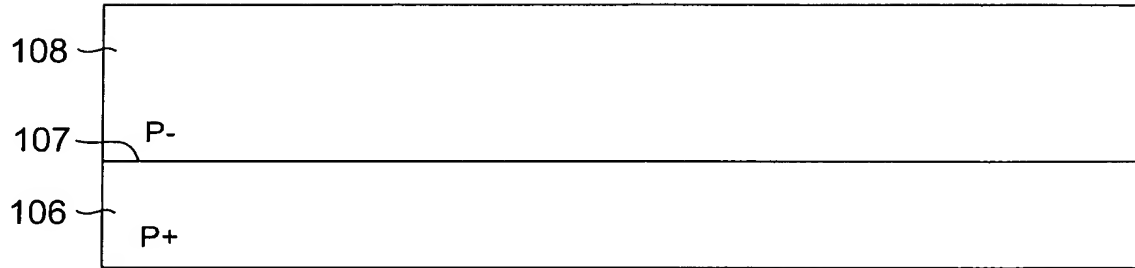


FIG. 3

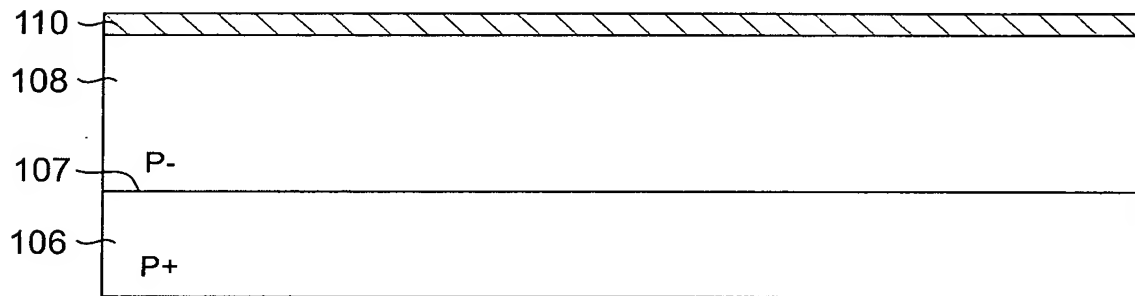


FIG. 4

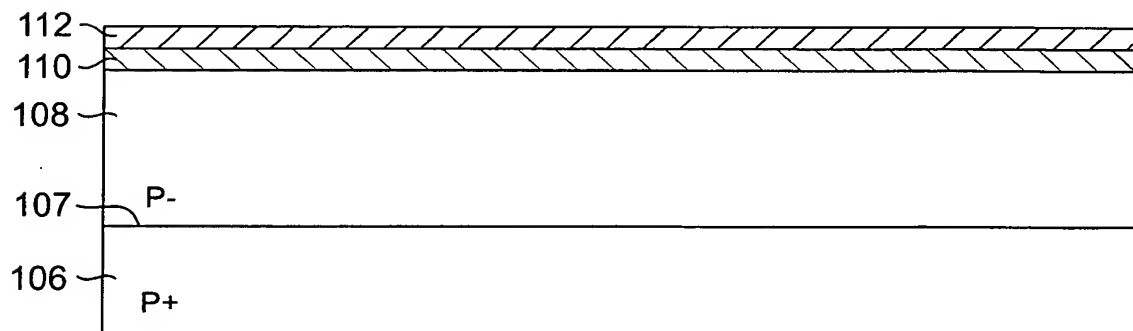


FIG. 5

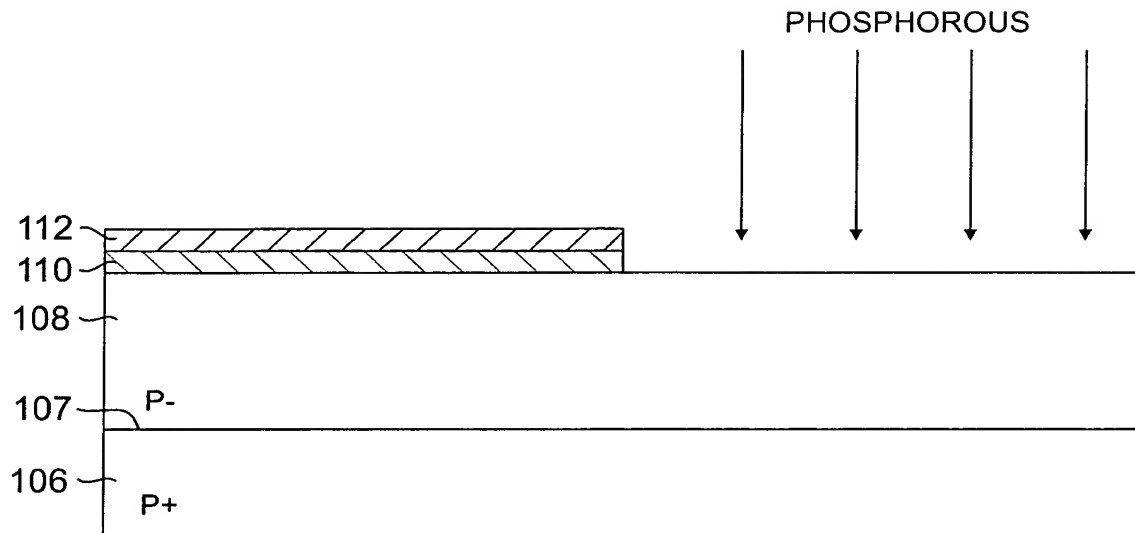


FIG. 6

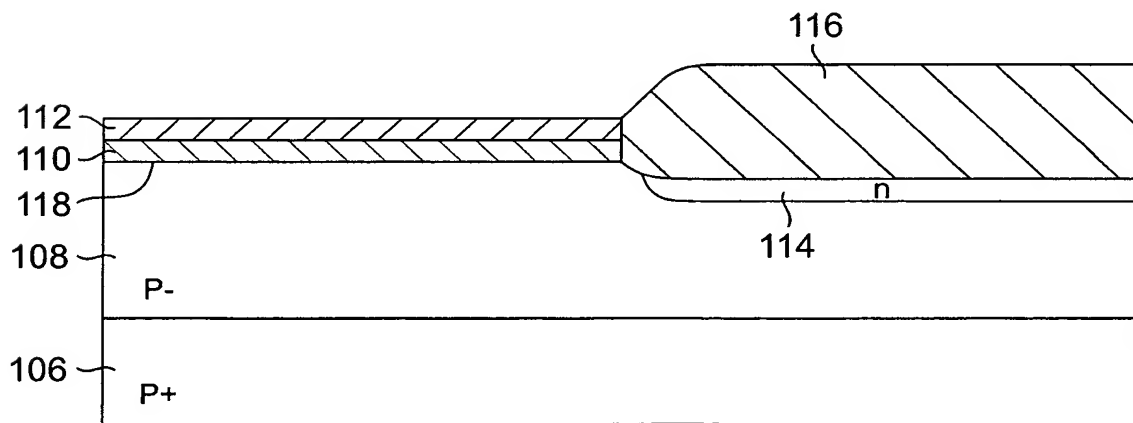


FIG. 7

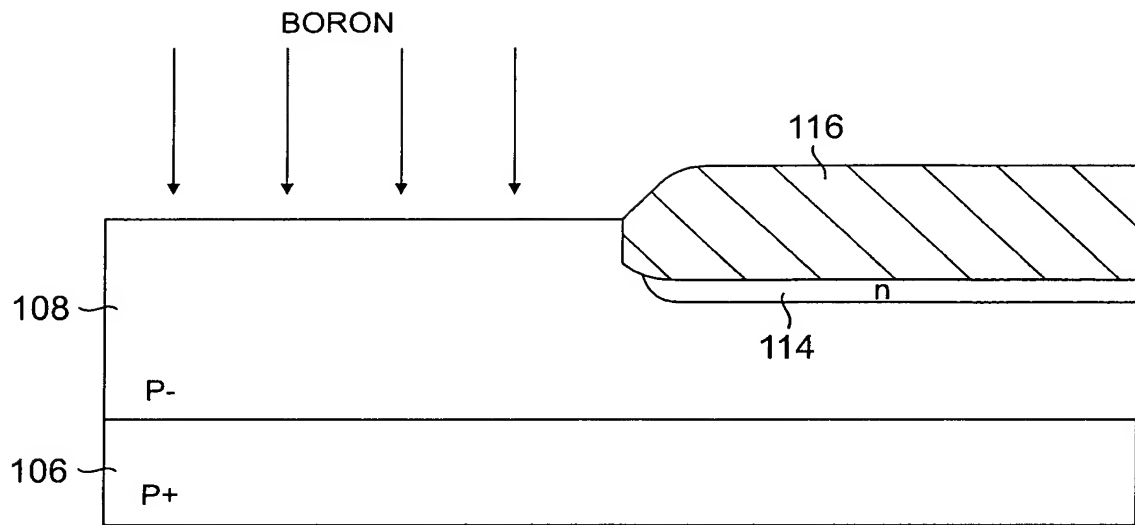


FIG. 8

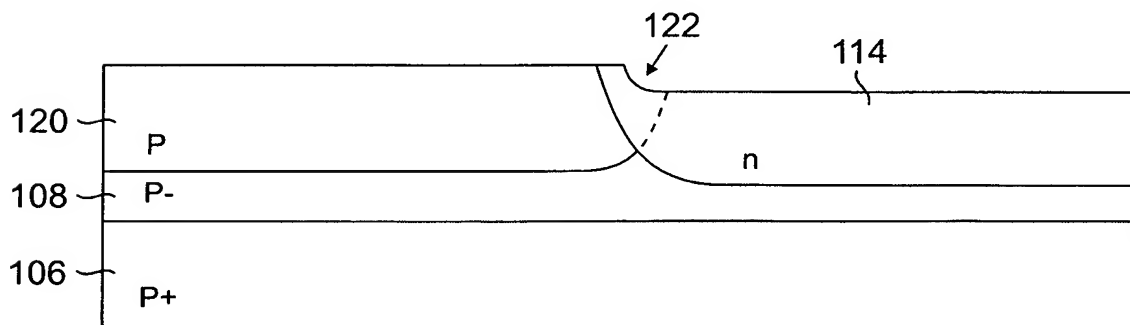


FIG. 9

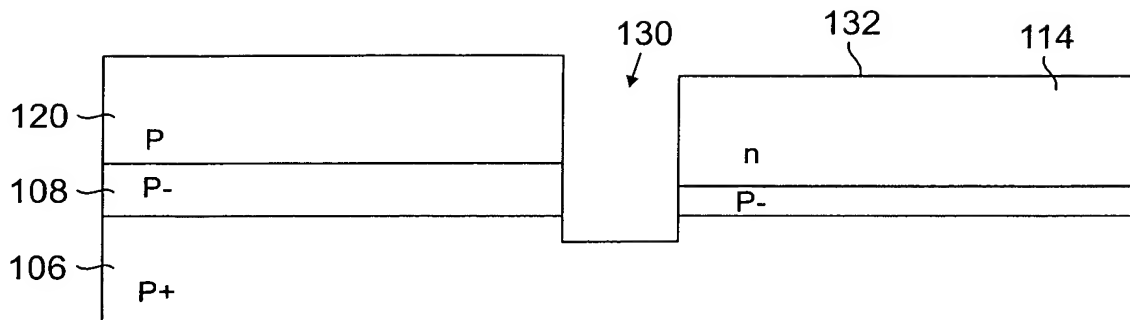


FIG. 10

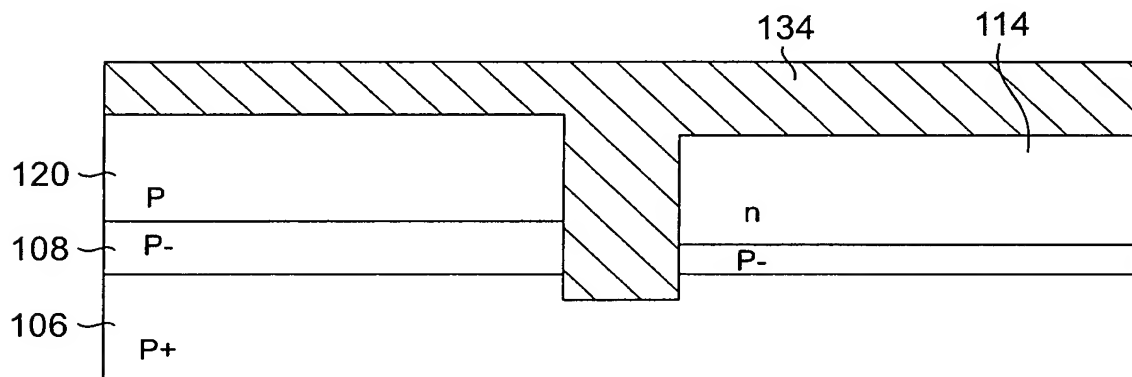


FIG. 11

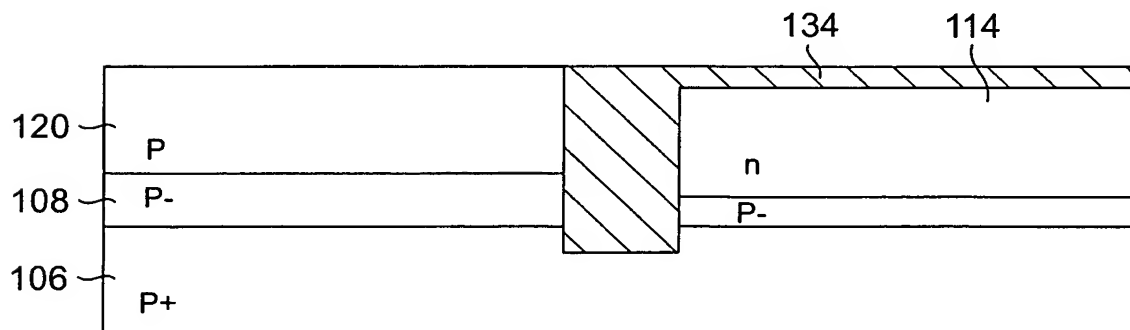


FIG. 12

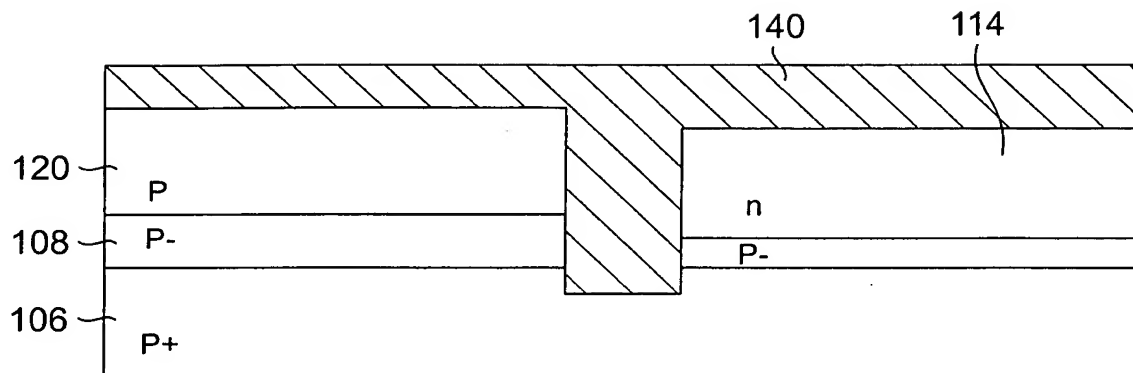


FIG. 13

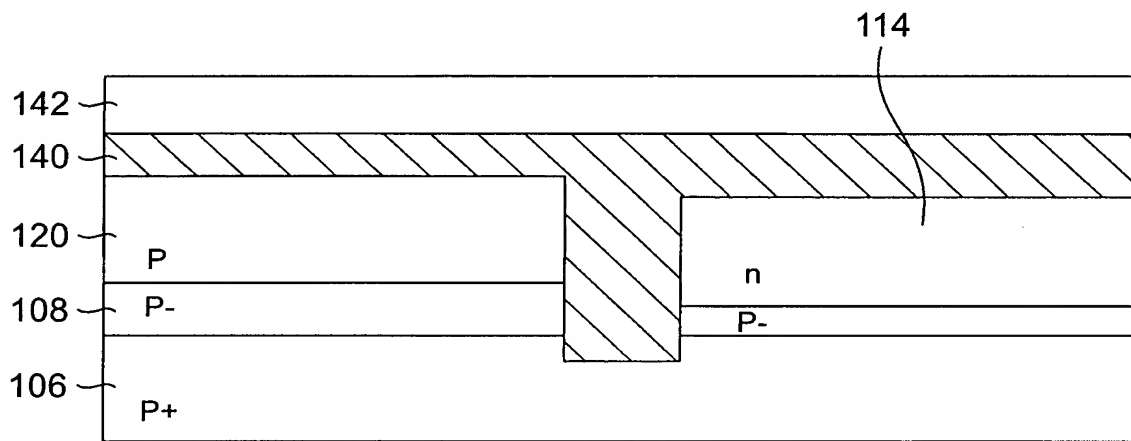


FIG. 14

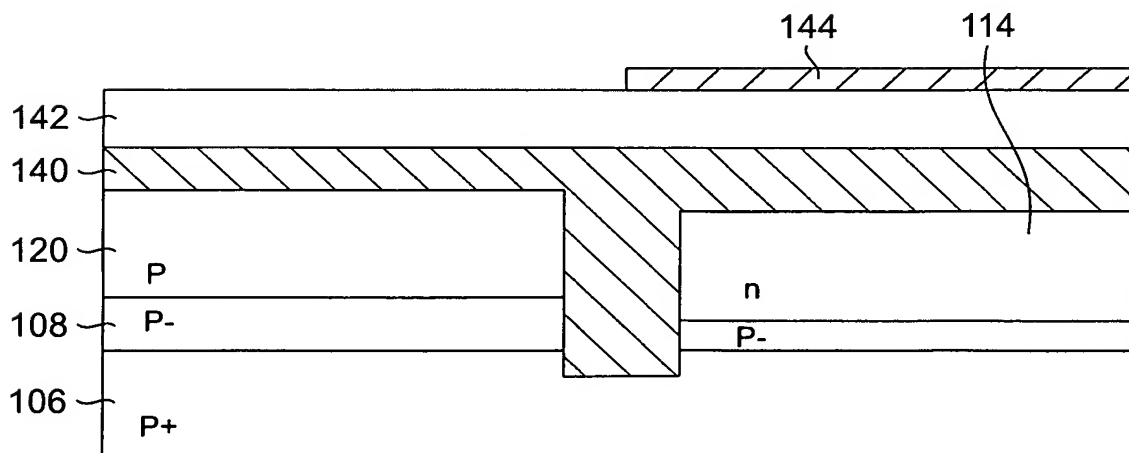
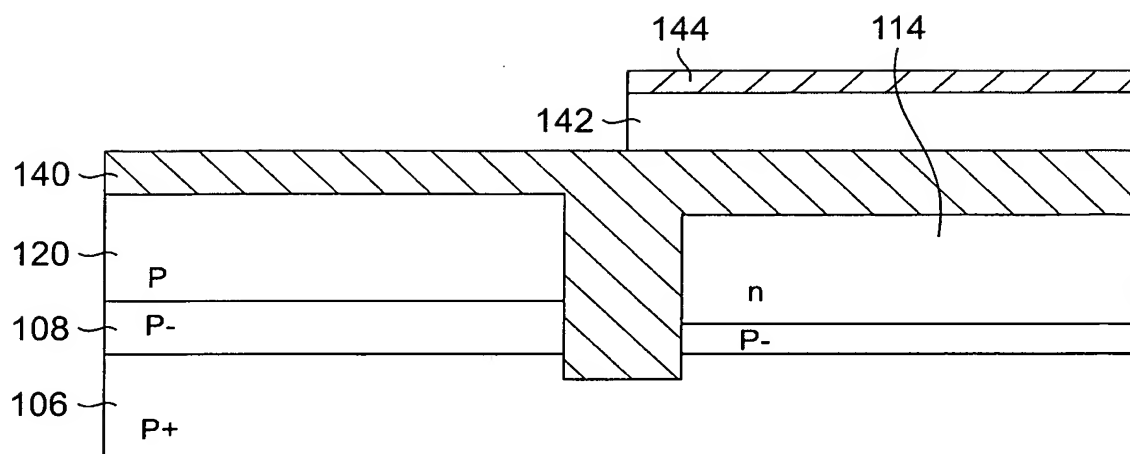


FIG. 15



This diagram shows a cross-sectional view of a semiconductor device. The structure includes a P+ emitter layer (106), a P- base layer (108), and a P collector layer (120). A P+ contact layer (140) is formed on the emitter. A P- layer (142) is formed on the base. A P+ layer (144) is formed on the collector. A P+ layer (146) is formed on the collector. A P- layer (114) is formed on the collector. The P+ layer (144) and P- layer (114) are formed on the P+ layer (146).

FIG. 17

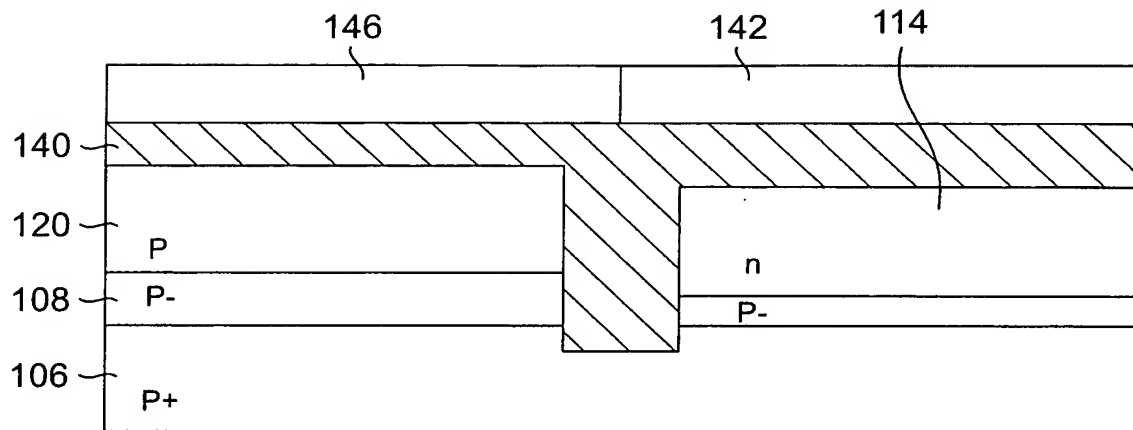


FIG. 18

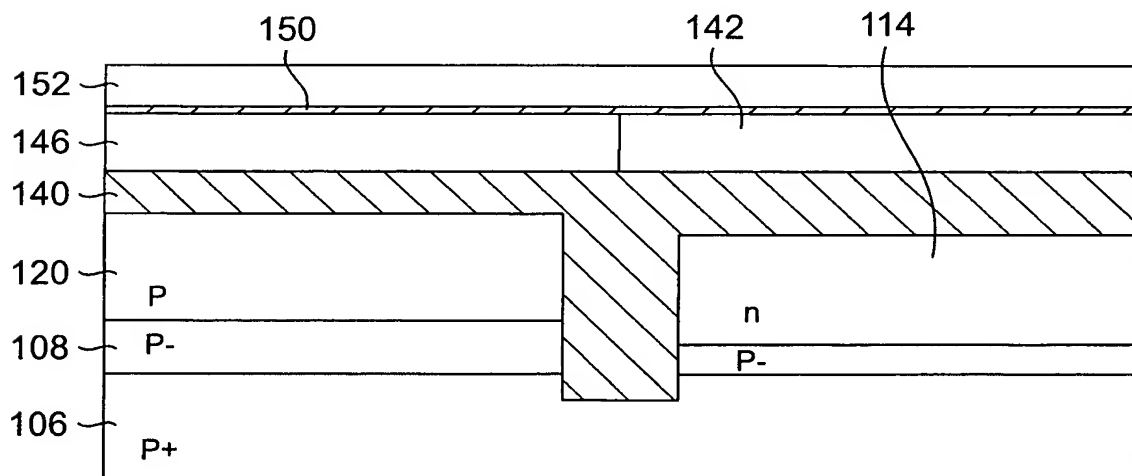


FIG. 19

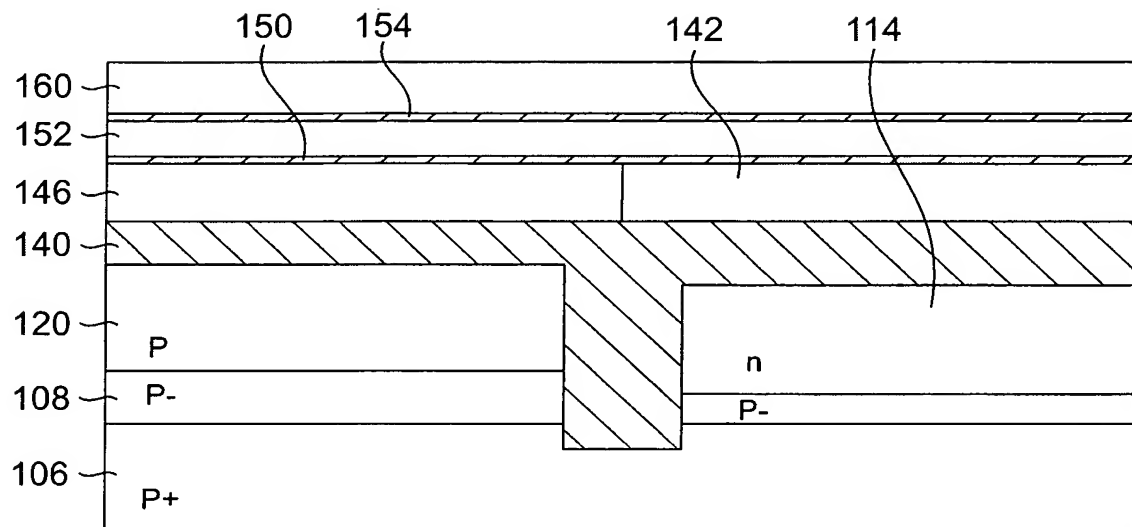


FIG. 20

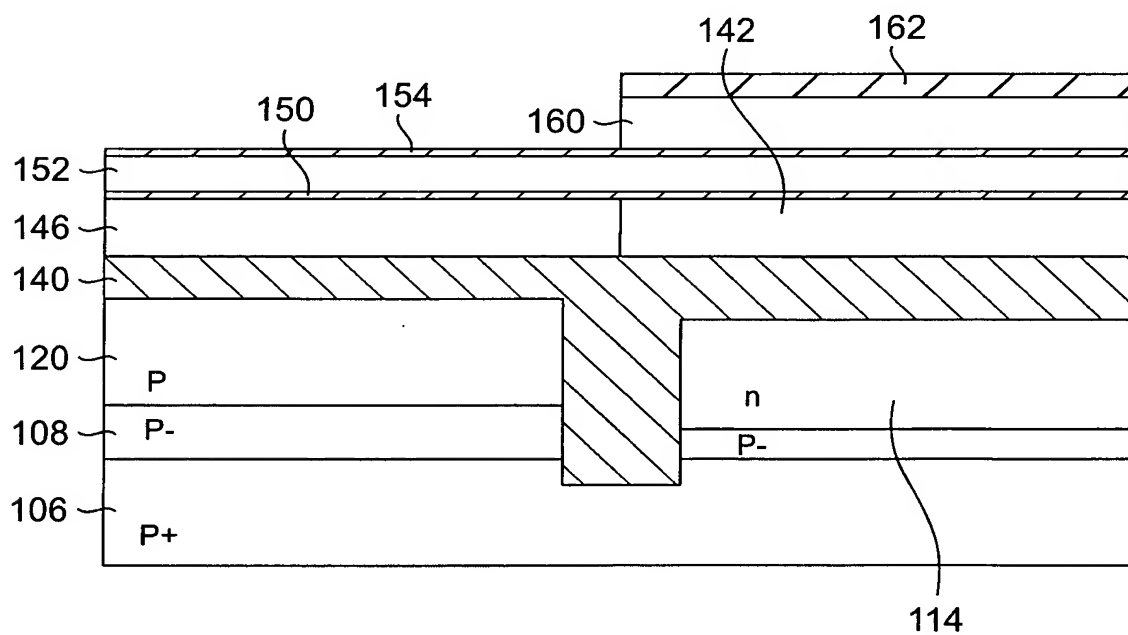


FIG. 21

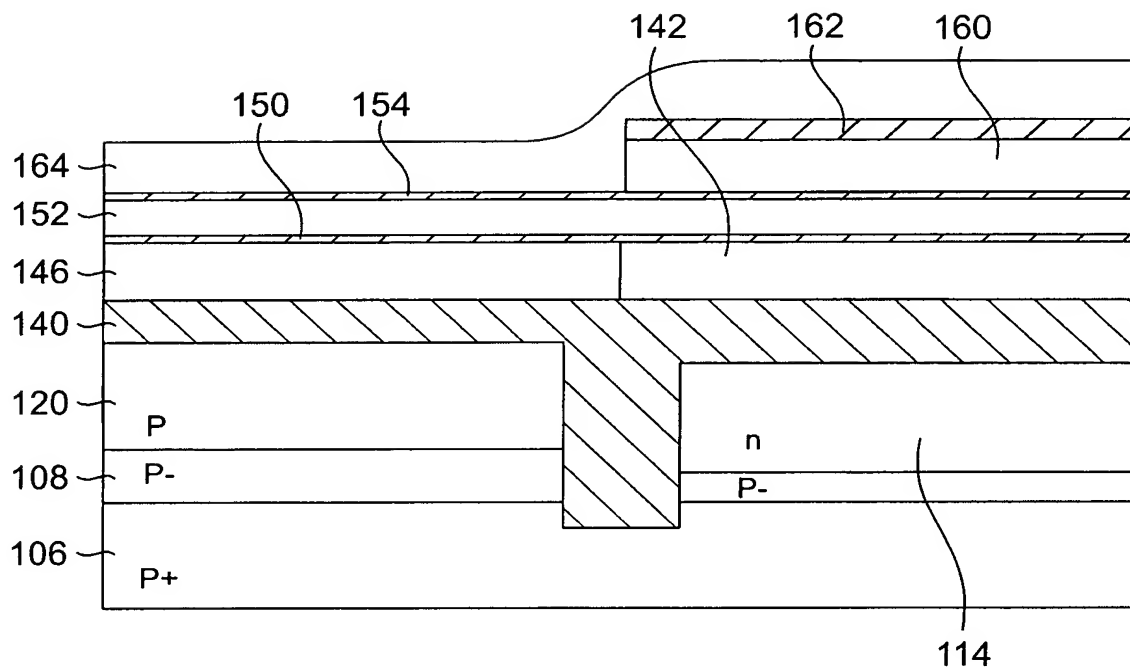


FIG. 22

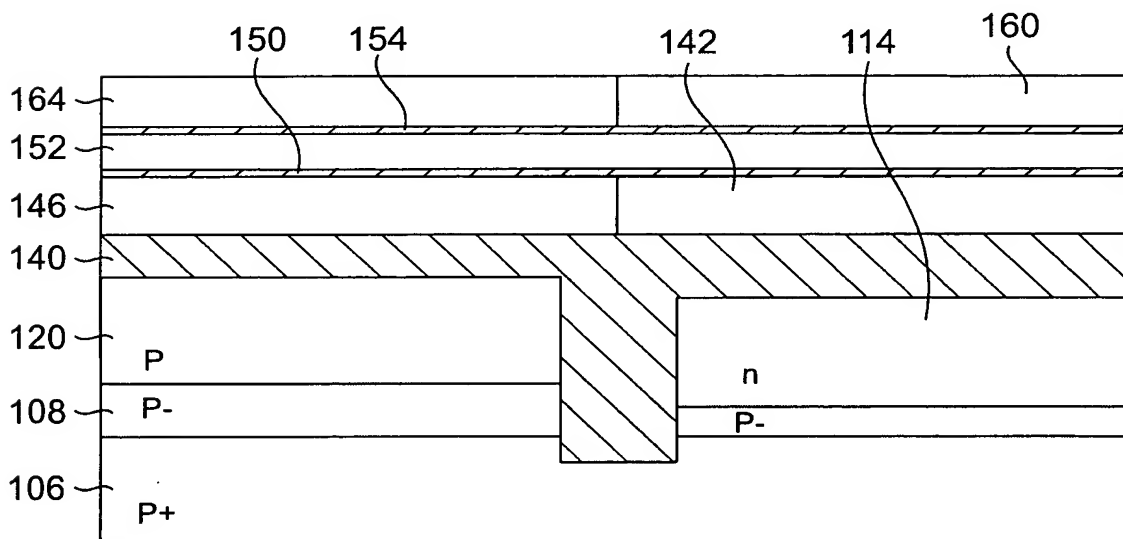


FIG. 23

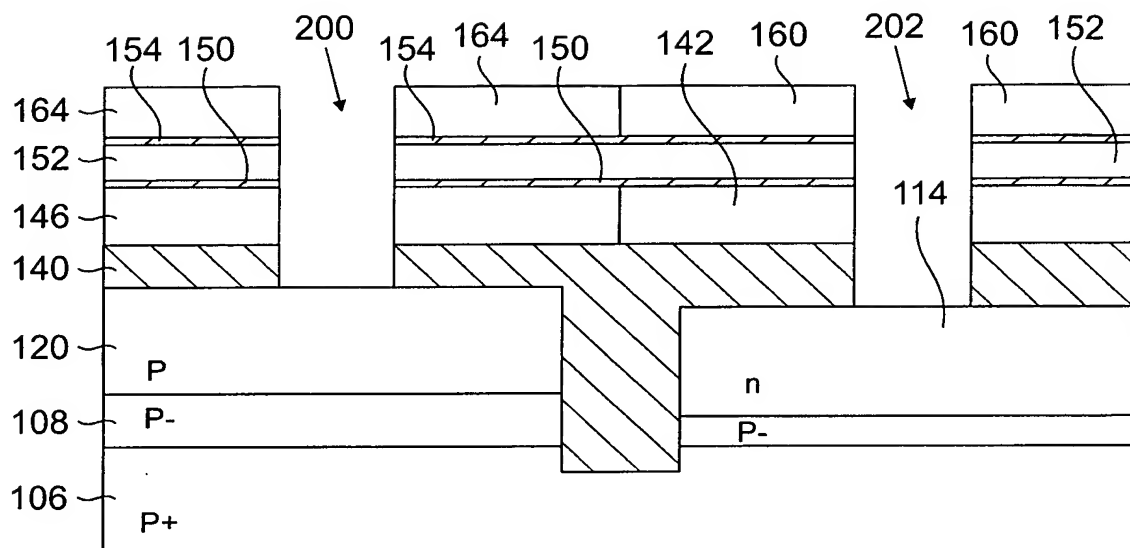


FIG. 24

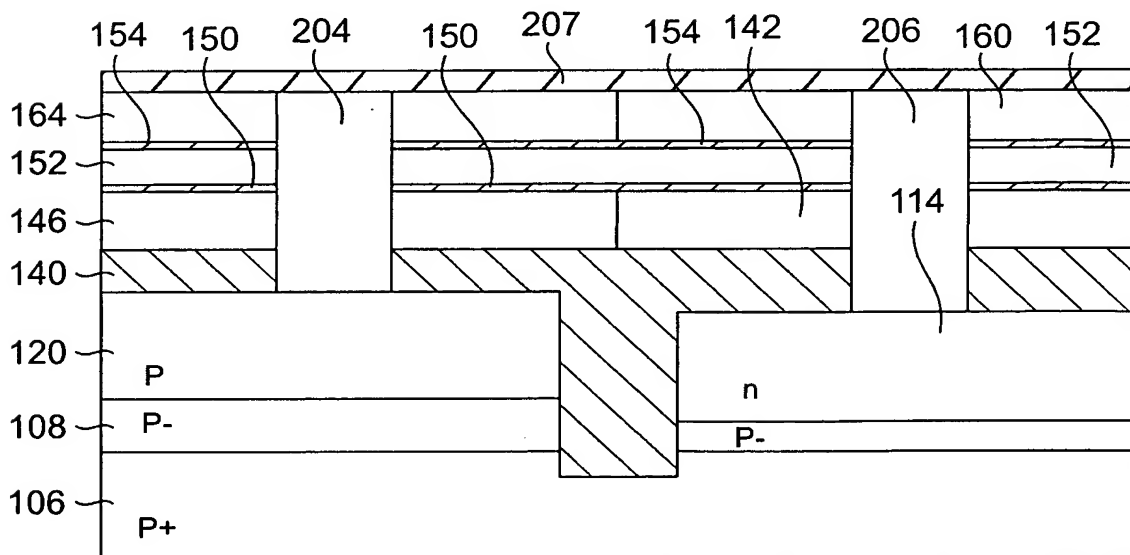


FIG. 25

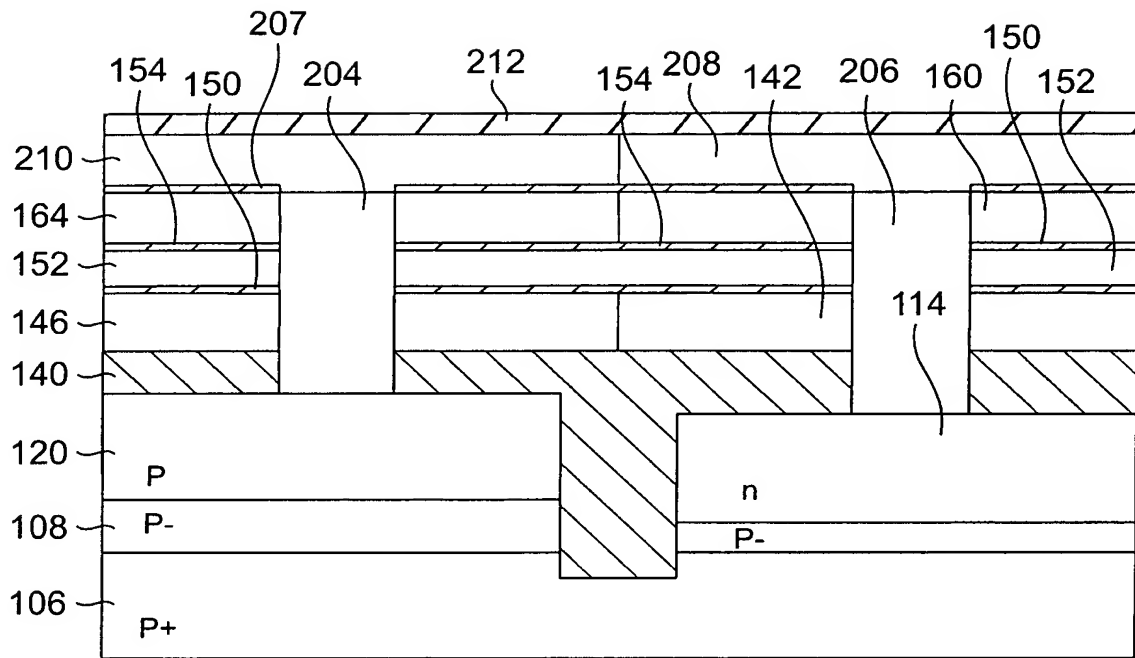


FIG. 26

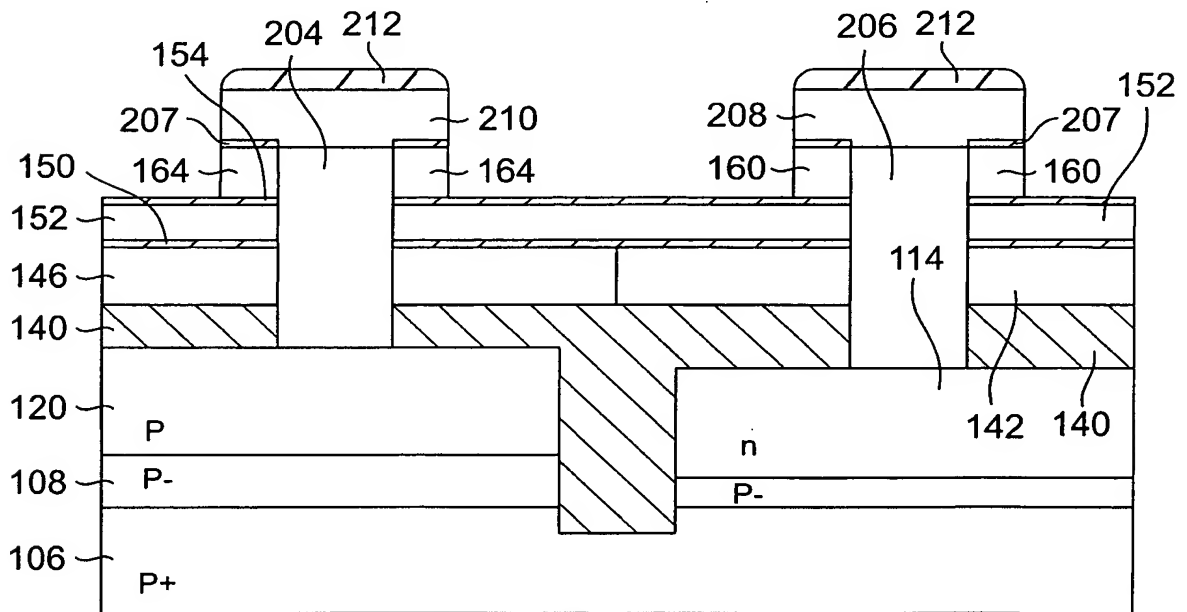


FIG. 27

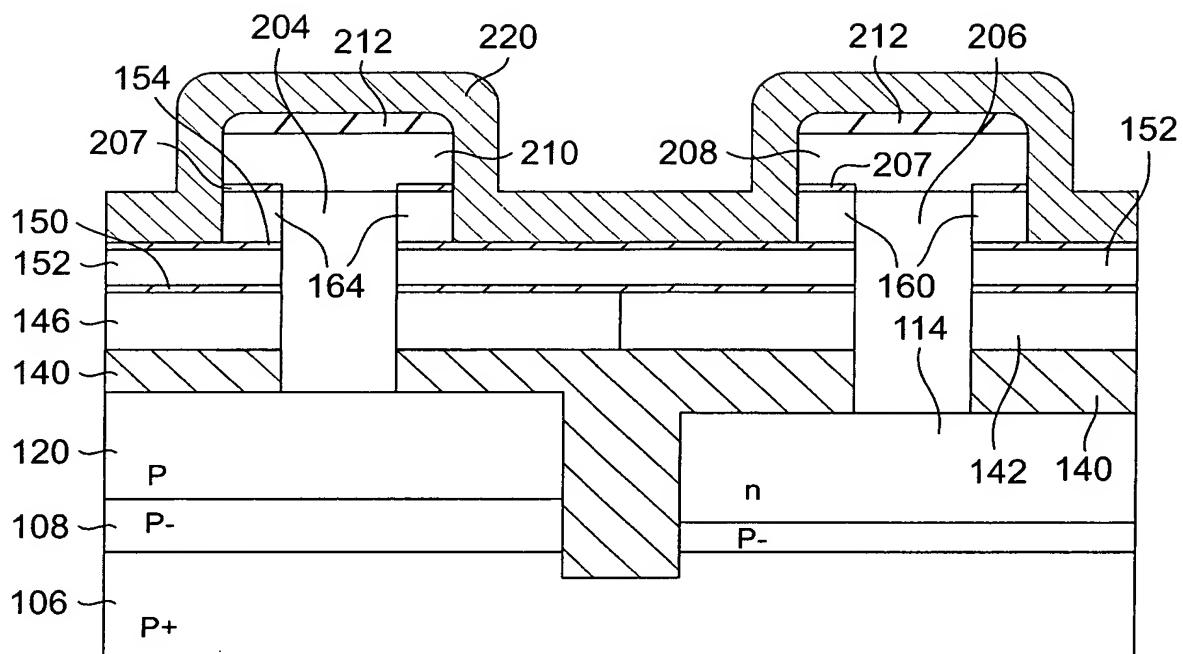


FIG. 28

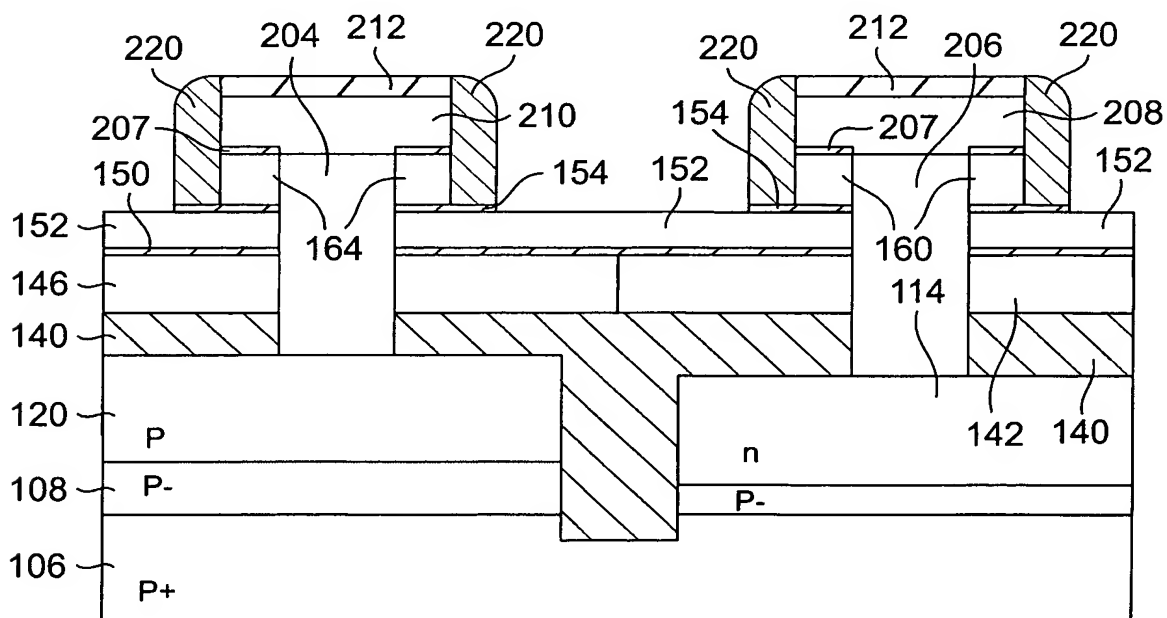


FIG. 29

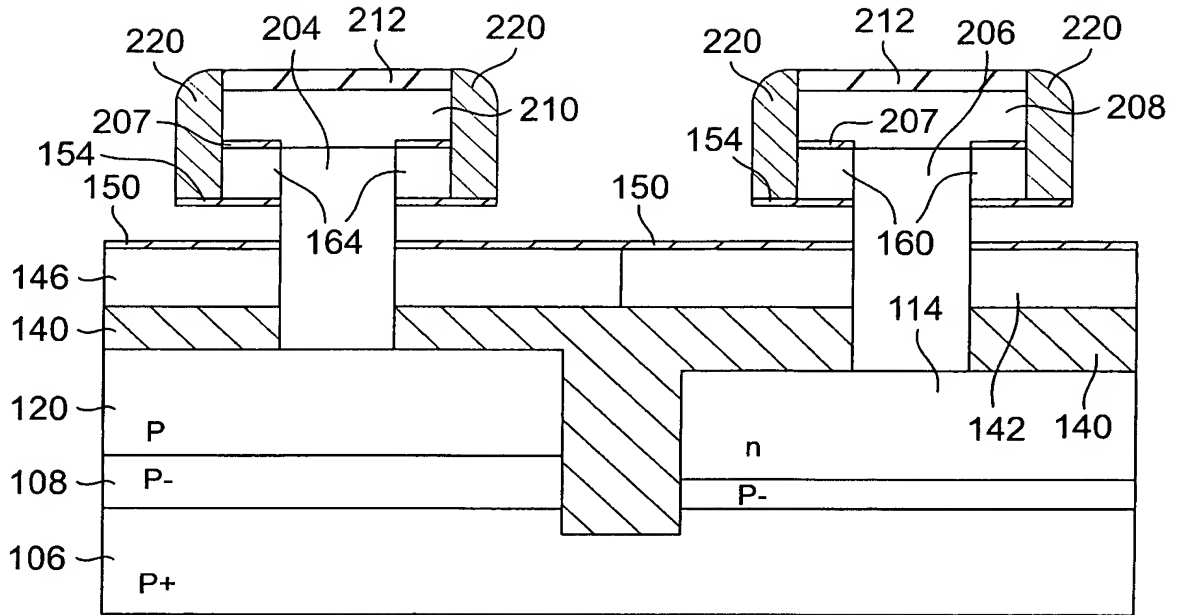


FIG. 30

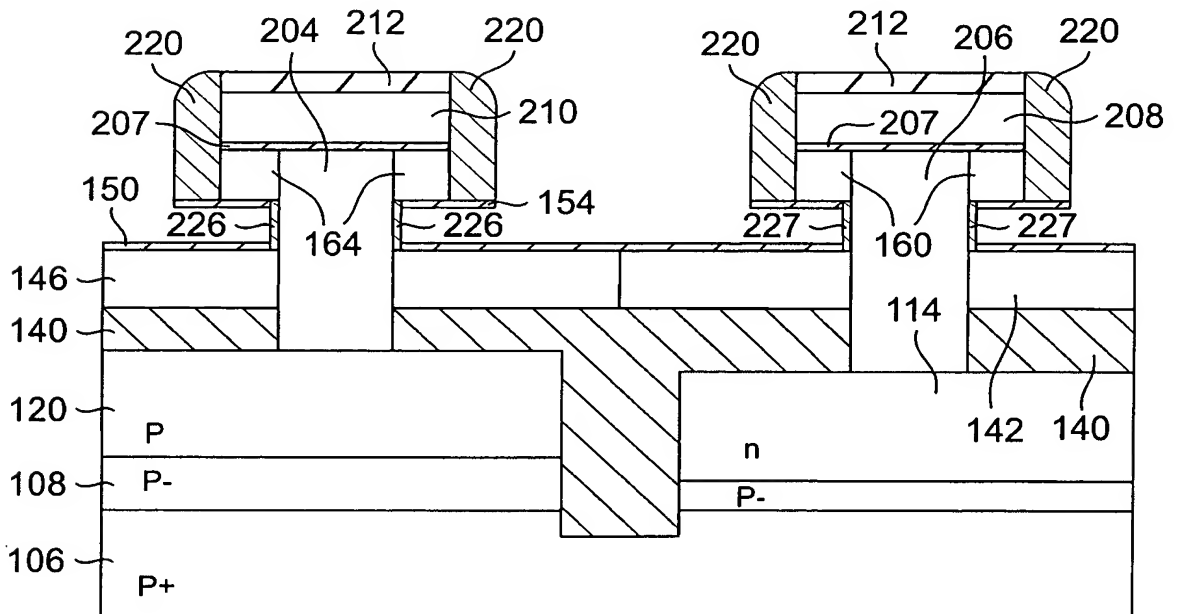


FIG. 31

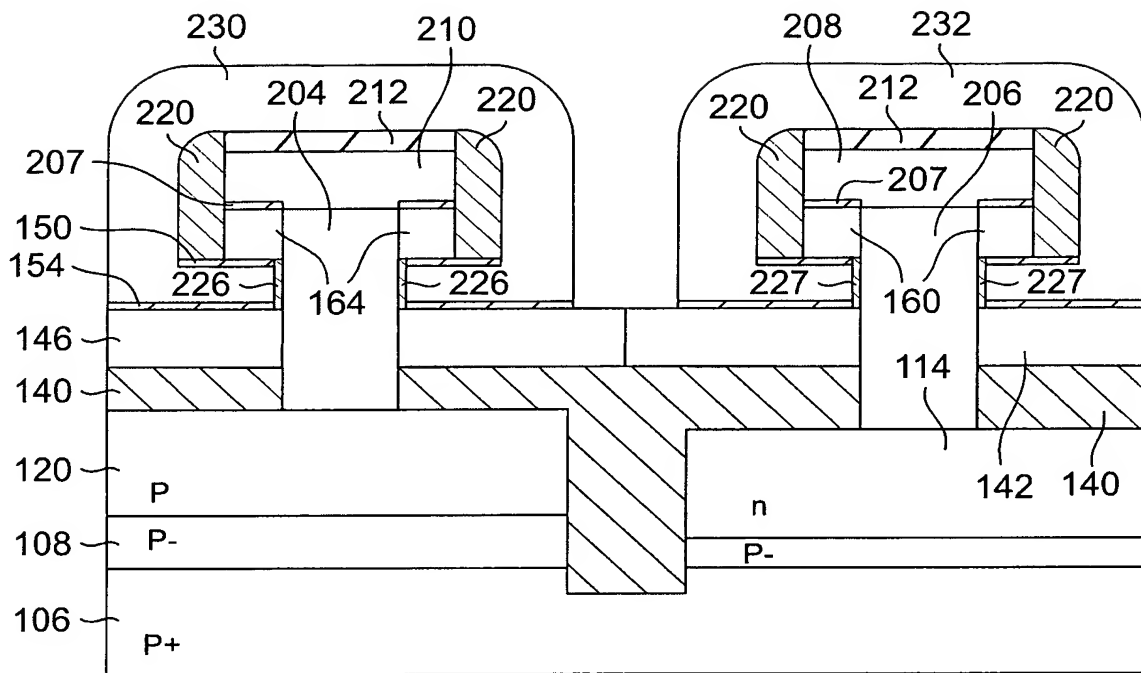


FIG. 32

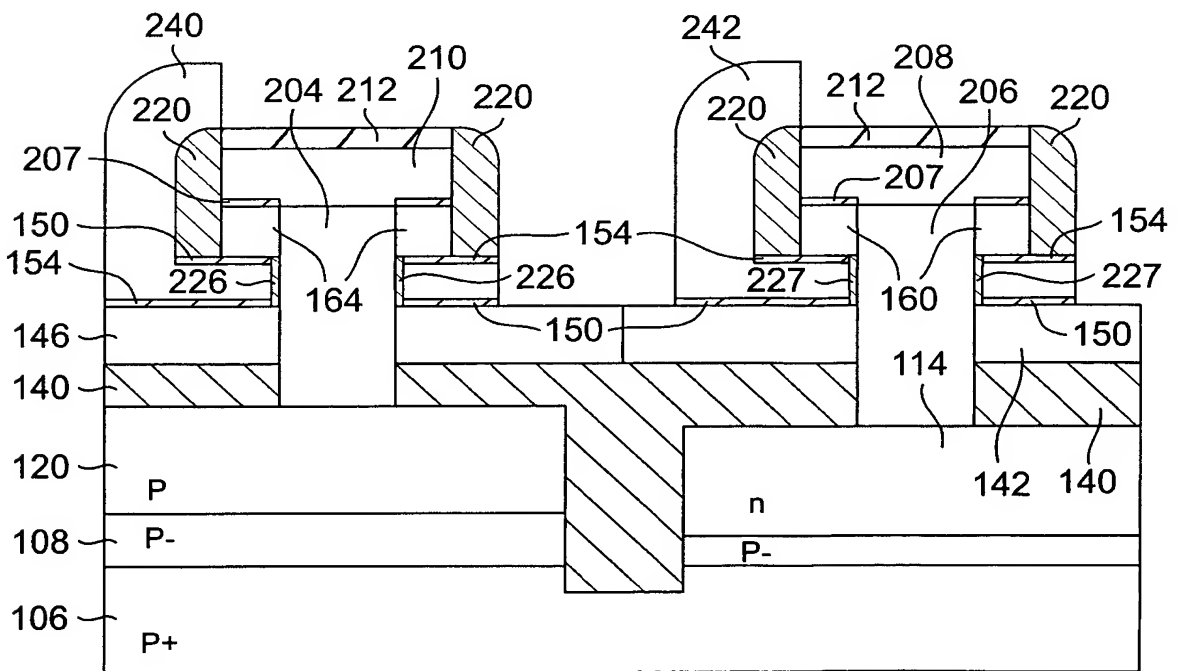


FIG. 33

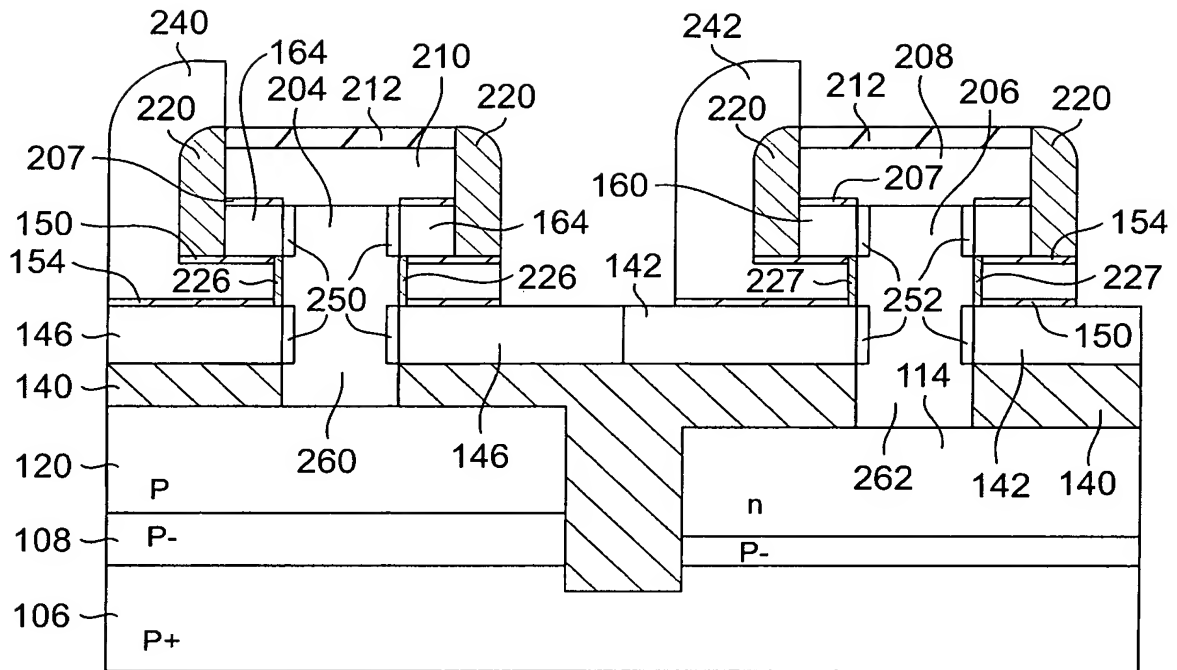


FIG. 34

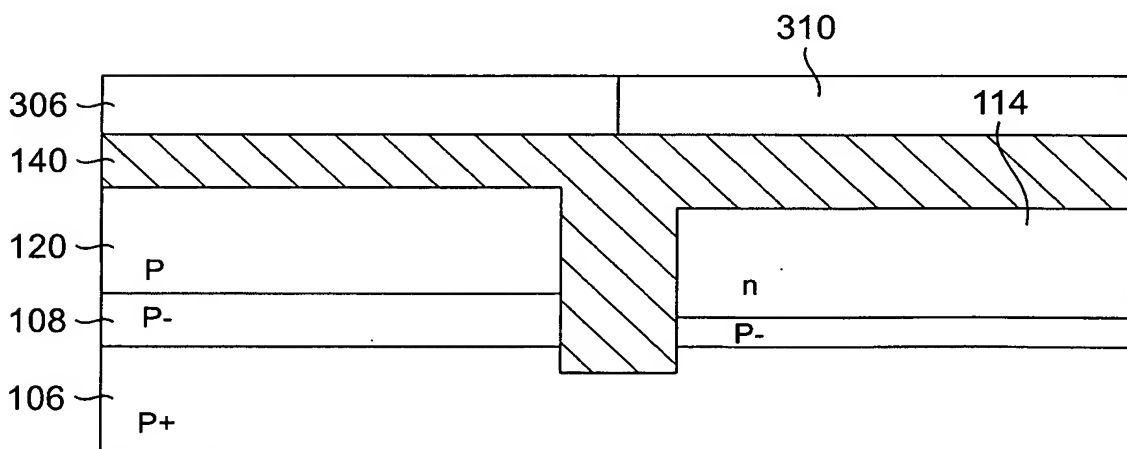


FIG. 40

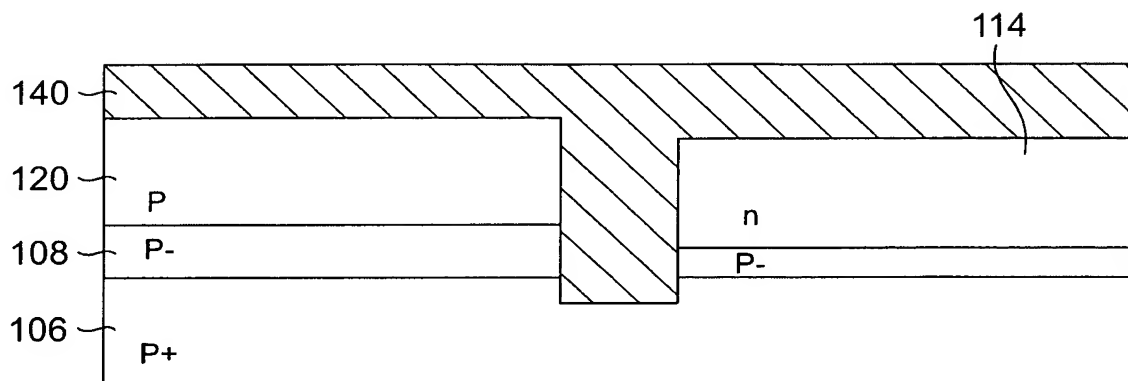


FIG. 35

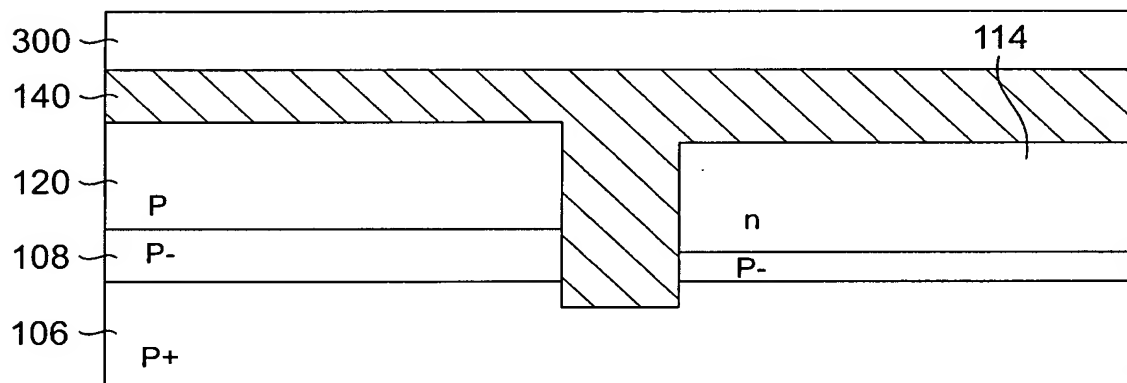


FIG. 36

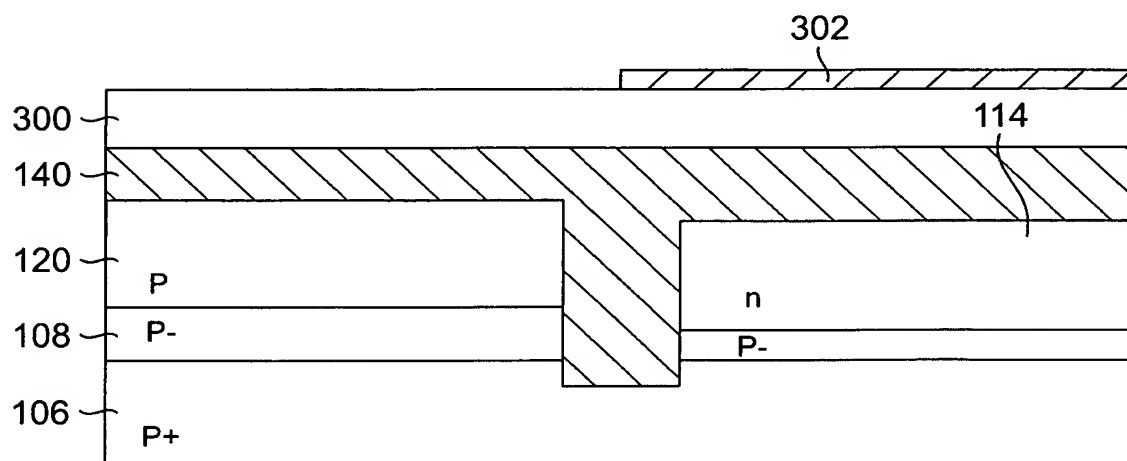


FIG. 37

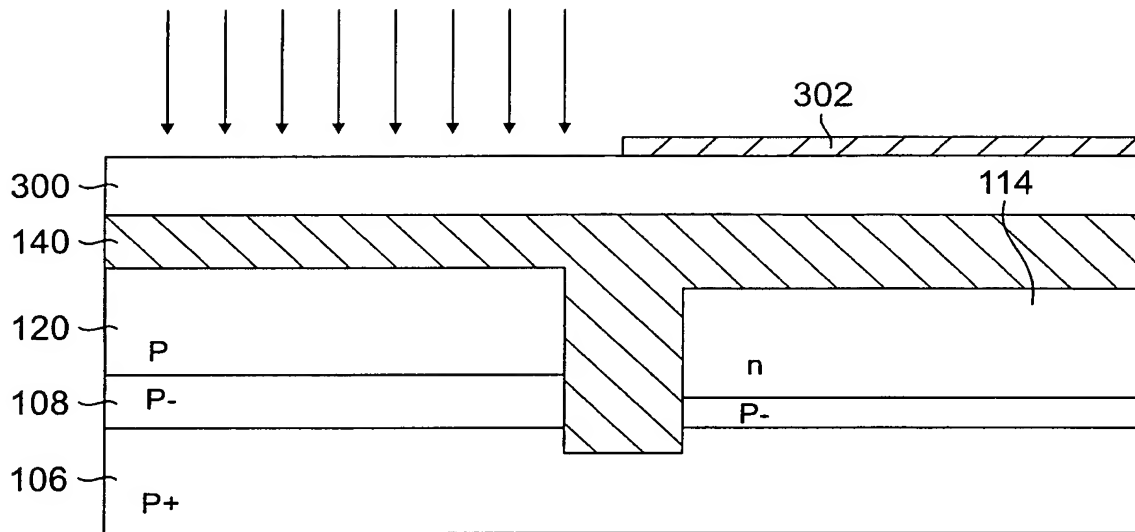


FIG. 38

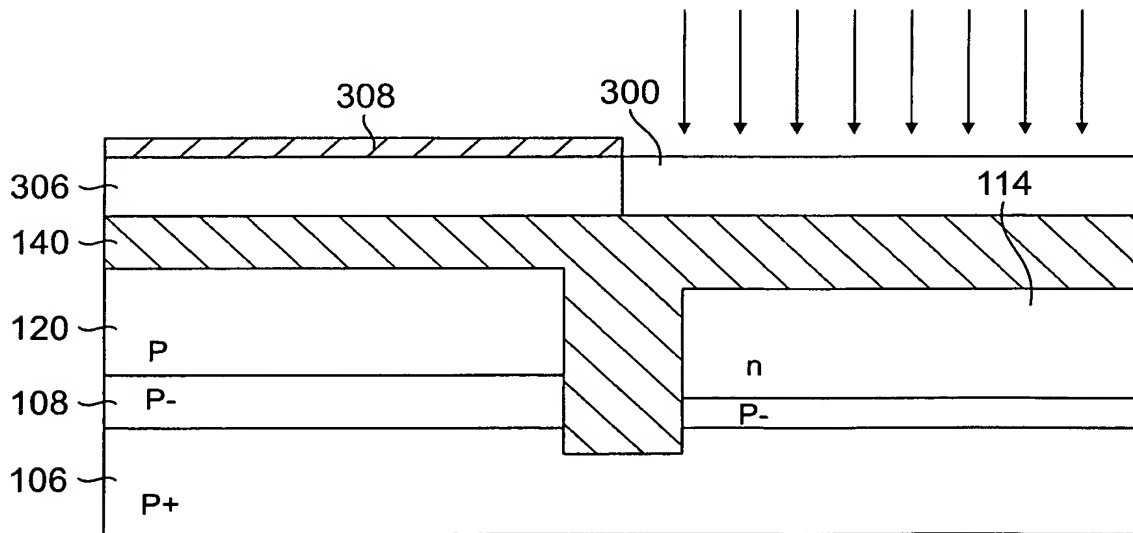


FIG. 39

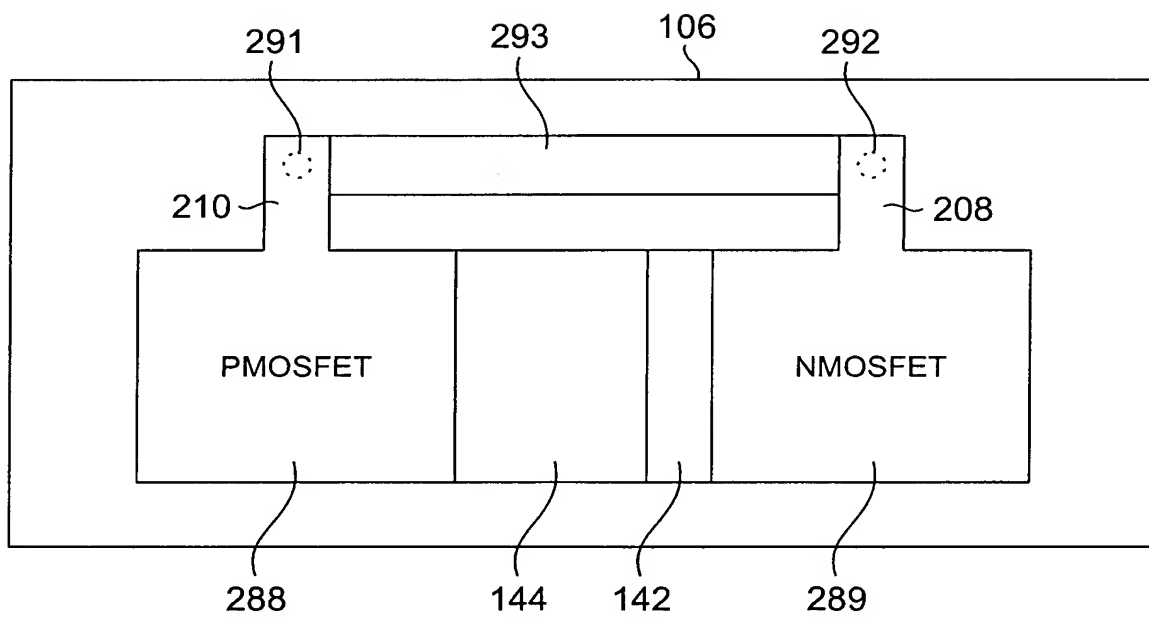


FIG. 41